Editorial

ON BEHALF OF the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (TVLSI), I wish you all a very Happy New Year 2004! Almost 11 months ago, I took over from Professor Eby Friedman, as the new Editor-in-Chief (EIC) of this journal. I understand the magnitude and significance of assuming such a responsibility and of my obligation to the readers, authors, reviewers, associate editors, publications staff, and the sponsoring societies of IEEE. It is extremely important to maintain and enhance the reputation of the journal. TVLSI has developed into a premier journal in the fields of design, analysis, and test of VLSI systems. The journal continues to grow in terms of quality and size, readership, submission, subscription, and impact. Along with the members of the new editorial board, we shall continue to strive towards providing the best service to the VLSI community.

First and foremost, I would like to express my sincere gratitude to the previous EIC, Prof. Friedman for his dedication and service to this journal, and for making my transition into the EIC position extremely smooth. On my request, Prof. Friedman agreed to continue as EIC for almost a month beyond his term so as to give me enough time to familiarize myself with TVLSI's publication system. Also, I thank him for being a gracious host during my visit to Rochester, NY, and for offering all the information and help I needed during the transition period. I record my gratitude to Ms. Ruth Ann Williams for her outstanding service and also for continuing to serve as the journal's editorial assistant for several additional months until I was able to hire a new editorial assistant.

I have an important announcement to share with the VLSI community. TVLSI will be published as a monthly publication starting January 2004, with an increased page budget of 1400 pages per year. This is a significant milestone for the IEEE TRANSACTIONS on VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and reflects the growing interest and demand for the journal. It took a lot of effort over the past few years to achieve the following: increasing the transactions' annual page budget from 744 to 1000 pages per year in 2002, increasing it to 1200 pages in 2003 and increasing it further to 1400 pages beginning in 2004, and also changing it into a monthly publication. We would like to express our gratitude to the TVLSI steering committee, and the Publications Boards of the sponsoring societies: IEEE Computer Society, IEEE Circuits and Systems Society and the IEEE Solid State Circuits Society. In particular, I would like to note with thanks the enthusiastic support I received from Dr. Peter Pirsch and Dr. M.N.S. Swamy of the IEEE Circuits and Systems Society, and Dr. Rangachar Kasturi, of IEEE Computer Society for their help in making a case for the increased page budget.

The steering committee of TVLSI plays an important role in framing the policies, debating on issues, and approving various activities related to the journal. I would also like to thank the past and current steering committee members such as Dr. Don Bouldin, Dr. Francky Cathoor, Dr. Eby Friedman, Dr. Peter Pirsch, and Dr. Wayne Wolf. The increased page budget and frequency of TVLSI directly impacts the staff at the IEEE Publications Office who dedicate enormous time and effort in formatting the articles, contacting the authors to return the proofs and copyright forms on time, and ensure the publication of the issue on time. TVLSI has had an enormous backlog in the recent years, which has been reduced to six or seven months by publishing very thick issues during the later part of 2002 and throughout 2003. We thank William A. Colacchio, Mona Mittra, Roena Rabelo Vega, Fran Zapulla, and the other staff members for their efforts in bringing TVLSI issues on schedule and absorbing the additional workload needed. The web system, Manuscript Central (MC), has gone through significant changes and improvements over time and many suggestions made by the associate editors have been incorporated. Special thanks are due to Sonal Parikh and Larry Perrone for their help with MC and the many suggestions by Dr. Bernard Courtois and Dr. Niraj K.Jha.

TVLSI continues to publish a few special sections embedded within an issue along with regular papers and briefs. The editorial board makes sure that the special section papers go through the same rigorous review process as the regular submissions and often the special sections, based on specific conferences, also welcome and consider submissions that were not included in the conference proceedings. Until we catch up with the backlog of regular papers, TVLSI will exercise caution in considering new proposals for special sections. In 2003, we published special sections based on conferences such as International Symposium on Low-Power Electronics and Design (ISLPED), International Conference on Computer Design (ICCD) and System-Level Interconnect Prediction (SLIP).

Another important announcement is the introduction of the position of Associate EIC for TVLSI starting January 2004. Such a position is common in most IEEE TRANSACTIONS of the magnitude of TVLSI and I am very pleased to announce that Dr. Srimat Chakradhar of the NEC Research Labs, Princeton, NJ, has kindly agreed to serve as the first Associate EIC of TVLSI. He has made significant research contributions in VLSI design, CAD, and test, has rich experience in terms of managing the review process for numerous large conferences, and has the credit of writing his own web-based system for conference program committee review management. As TVLSI is becoming a monthly publication in 2004, with an increased page budget and, thus, an increased number of submissions, the Associate EIC will help towards sharing the load and in handling papers that involve any type of conflicts of interest.

I am extremely proud to introduce the current editorial board for TVLSI. They have played a tremendous role in the background towards the smooth operation of TVLSI, significantly improving the timeliness of the review process. The statistics presented in Table I will speak volumes of their efforts. Their

Digital Object Identifier 10.1109/TVLSI.2003.822591

TABLE I
TABLE SHOWING STATUS OF TVLSI: STATISTICS AND REVIEW TIMELINES

TVLSI status summary	2001	2002	2003 (as of 10/31/03)
No. of manuscripts submitted:	353	373	379
No. of manuscripts accepted:	82	123	83
No. of manuscripts rejected:	93	86	79
No. of manuscripts still under review:	0	16	115
Backlog of accepted papers (months):	10–12	11–14	5–7
No. of papers published:	93	94	112
Annual Page budget:	744	1000	1200
No. of printed pages:	1000	965	1180
Review process timeline (average no. of days*)			
Submission to EIC:	2	1	0.6
EIC to AE assignment:	18	8	9
AE request to Reviewer agreement:	50	44	20
Reviewer agreement to AE recommendation:	108	95	72
AE recommendation to EIC decision:	15	11	7
Submission to decision:	193	159	109
Decision to revised submission (delay by author):	119	162	193
Initial submission to final decision including author delay:	312	321	294
*averaged for all submissions processed during the year			

biographies and photographs are presented in the pages following this editorial. In line with the increase in the number of submissions, we have increased the number of associate editors. On behalf of TVLSI, I express my deepest gratitude to all the associate editors, both who have completed their terms and those currently serving, for their contributions. It is needless to mention the reviewers who play the ultimate role in the review process with providing the indepth technical reviews—volunteering their precious time. I offer my sincere thanks to each and every reviewer for their reviews as well as for their patience regarding the constant reminder emails generated by both the system and my editorial assistant, Michael Pham. If I perform my responsibilities well, a large part of the credit goes to Michael for all his efforts. I have been extremely fortunate in finding the best person suitable for the position. He is extremely meticulous, organized, sincere and hardworking, and his efforts have been phenomenal in terms of tracking the review process.

A word to authors regarding the time it takes to resubmit their revised manuscripts: as we look at the table of timelines for the review process, a glaring problem is the average delay by the authors in resubmitting the revised manuscripts. The current numbers are unacceptable and the editorial board is making a strict policy in terms of the time taken by the authors in submitting the revised manuscripts. We request the authors to strictly adhere to the given time limits (typically, four to six weeks for a regular paper and three to four weeks for a transaction brief). In deserving cases, where the required major revisions need more time, the author can request by emailing the associate editor (copying the EIC) for additional time with justification. This is important for continuity of the review process and for the reviewer, who will still remember to some extent the main ideas described in the paper.

While we have significantly improved the review process timelines, there is room for improvement starting from the EIC front. We will continue to strive to improve as much as possible. There are always a few papers that get delayed beyond acceptable times, and we are beginning to understand how to track and avoid such problems. The amount of emails that arrive each day at the EIC center (tvlsieic@csee.usf.edu) is quite large and we are trying as best as we can to take care of the problems. After all, the success of the journal is mainly due to the collective efforts of all the players: the EIC, the associate editors, the reviewers, and the authors. We are always open to suggestions!

NAGARAJAN (RANGA) RANGANATHAN, *Editor-In-Chief*
Prof. of Computer Science and Engineering
Nanomaterials and Nanomanufacturing Research Center
University of South Florida
Tampa, Florida 33620

Nagarajan (Ranga) Ranganathan (S'81–M'88–SM'92–F'02) received the B.E. (Hons.) degree in electrical and electronics engineering from the Regional Engineering College, Tiruchirapalli, University of Madras, India, in 1983, and the Ph.D. degree in computer science from the University of Central Florida, Orlando, in 1988.

He is currently a Professor in the Department of Computer Science and Engineering and with the Nanomaterials and Nanoelectronics Research Center at the University of South Florida, Tampa. From 1998 to 1999, he was a Professor at the University of Texas, El Paso. His research interests include VLSI design, design automation, computer architecture, and parallel processing. His recent research has focused on dynamic power estimation and optimization, leakage power reduction, and low power synthesis. He has developed many special purpose VLSI chips for computer vision, image processing, pattern recognition, data compression and signal processing applications. He has published over 175 papers in reputed journals and conferences and is a co-owner of five U.S. patents.

Dr. Ranganathan is a Member of the IEEE Computer Society and IEEE Circuits and Systems Society. He served on the editorial boards for the journals: *Pattern Recognition* from 1993 to 1997, *VLSI Design* from 1994 to the present, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS from 1995 to 1997, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING from 1997 to 1999, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY from 1997 to 2000. He was the Chair of the IEEE Computer Society Technical Committee on VLSI from 1997 to 2001. He served as the Steering Committee Chair of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS from 2001 to 2002, and is now serving as the Editor-in-Chief for 2003–2004. Recently, he received the Theodore and Venette Askounes–Ashford Distinguished Scholar Award at the University of South Florida, Tampa.

Srimat T. Chakradhar (S'88–M'88) received the Ph.D. degree in computer science from Rutgers University, New Brunswick, NJ, in 1990.

He is currently a Department Head at NEC Laboratories America, Inc., Princeton, NJ. In 1989, he was with AT&T Bell Laboratories, Murray Hill, NJ. His current research interests include design and test of hardware and software for networked computing systems, electronic design automation, wireless and embedded systems, and system-on-a-chip designs. He has published one book, over 100 technical papers in refereed journals and conference proceedings, and has been awarded more than 50 U.S. and international patents (Japan and Europe) in computing systems software and hardware. He has also served as a thesis advisor for four Ph.D. dissertations from reputed Universities.

Dr. Chakradhar has received five Best Paper Awards and four Award Nominations at premier international conferences of the ACM and IEEE for his work on design and test of computing systems. He has successfully organized and served on the board of several international conferences organized by the ACM or IEEE, in various capacities including General Chair and Technical Program Chair. He has served as Guest Editor for numerous IEEE publications and he is presently the Associate Editor for the *Journal on Electronic Testing*.

Vishwani D. Agrawal (S'68–M'70–SM'80–F'86) received the B.E. degree from the University of Roorkee, Roorkee, India, in 1964; the M.E. degree from the Indian Institute of Science, Bangalore, India, in 1966; and Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign, in 1971.

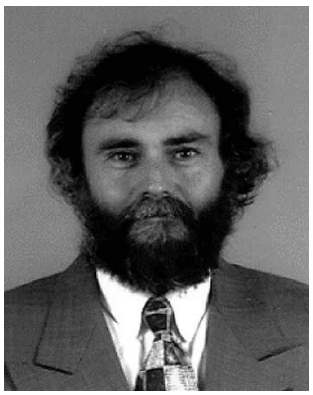
Currently, he is an Adjunct Visiting Professor with the Department of Electrical and Computer Engineering, Rutgers University, New Brunswick, NJ, a position he has held since 1990. He recently retired from Agere Systems to pursue a full-time academic and consulting career. He has over 30 years of industry and university experience, working at Bell Labs, Murray Hill, NJ; Rutgers University, New Brunswick, NJ; TRW, Redondo Beach, CA; IIT, Delhi, India; EG&G, Albuquerque, NM; and ATI, Champaign, IL. He has published over 250 papers, coauthored five books and has 13 U.S. patents. He is coauthor of *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits* (Norwell, MA: Kluwer, 2000). His research areas of expertise include VLSI testing, low-power design, and microwave antennas. Intensely interested in education and research, he serves on the Advisory Boards of the Electronics and Computer Engineering Departments of the University of Illinois, Urbana–Champaign, and the New Jersey Institute of Technology, Newark; he also teaches at Rutgers University, and has directed the Ph.D. thesis research of students at various universities including University of California, Berkeley, Carnegie Mellon University (CMU), Pittsburgh, PA, Univerity of Nebraska, Lincoln, Rutgers University, and the University of Wisconsin, Madison.

Dr. Agrawal is Founder and Editor-in-Chief of the *Journal of Electronic Testing: Theory and Applications*, since 1990. From 1985 to 1987, he was Editor-in-Chief of the *IEEE Design & Test of Computers Magazine*. He is the Founder and Consulting Editor of the *Frontiers in Electronic Testing* Book Series of Kluwer Publisher, Norwell, MA. He is a Cofounder of the International Conference on VLSI Design, and the International Workshops on VLSI Design and Test, held annually in India. He has served on numerous conference committees and is a frequently invited speaker. He was the invited Plenary Speaker at the 1998 International Test Conference, Washington, D.C., and the Keynote Speaker at the 9th Asian Test Symposium, held in Taiwan, in 2000. During 1989 and 1990, he served on the Board of Governors of the IEEE Computer Society. He has received seven Best Paper Awards and one Honorable Mention Paper Award. In 1998, he received the Harry H. Goode Memorial Award of the IEEE Computer Society for "innovative contributions to the field of electronic testing," and in 1993, he received the Distinguished Alumnus Award of the University of Illinois at Urbana-Champaign, "in recognition of his outstanding contributions in design and test of VLSI systems." In 1983, he was elected Fellow of IETE-India, and in 2003, he was elected Fellow of the ACM.

Travis Blalock received the B.S.EE (Hons.) and M.S.EE degrees, from the University of Tennessee, Knoxville, in 1985 and 1988, respectively, and the Ph.D. degree from Auburn University, Auburn, AL, in 1991.

Dr Blalock joined the Faculty of the Department of Electrical and Computer Engineering, University of Virginia, in 1988. He has published over 15 technical articles and holds or has pending 12 patents in the area of mixed-signal CMOS integrated circuit design. He was previously with Hewlett-Packard Laboratories, where he worked as a Principal Project Scientist. While at Hewlett-Packard he was the Lead Designer on several mixed-signal CMOS integrated circuits, including an analog discrete-time delay line for magnetic recording channels, an image detector with an on-chip parallel cross-correlation processor for position encoding, and an analog silicon backplane for a high-resolution microdisplay. His primary research interests include CMOS digital and analog signal processor design, low-power analog/digital converter design, integrated optoelectronic sensors and signal processing, and low-power architectures for human-computer interfaces. Other interests include built-in self-test for analog integrated circuits, low-voltage feedback amplifiers, reference circuits, analog neural networks, multilevel digital logic, infinite persistence analog sample-and-hold circuits, high-efficiency on-chip voltage converters, and mixed-signal CAD techniques.

He is a Member of Eta Kappa Nu, Sigma Xi, and Tau Beta Pi.



Bernard Courtois received the Engineer degree in 1973 from the Ecole Nationale Supérieure d'Informatique et Mathématiques Appliquées de Grenoble, France, and the Docteur-Ingénieur and Docteur-ès-Sciences degrees from the Institut National Polytechnique de Grenoble, France.

He is currently Director of the Laboratory of Techniques of Informatics and Microelectronics for Computer Architecture (TIMA), where his research interests includes CAD, architecture, and testing of integrated circuits and systems. He is also the Director of the CMP Service that is servicing universities and companies from about 60 countries for ICs, MCMs, and MEMS prototyping, and small volume production.

Dr. Courtois has been the General Chair or Program Chair of various international conferences and workshops, including EDAC-ETC-EUROASIC, Electron and Optical Beam Testing, EUROCHIP, Mixed-Signal Testing, Rapid System Prototyping, THERMINIC, Design, Test and Microfabrication of MEMS/MOEMS and Polytronic. He is a Member of ACM, ASME, and IMAPS. He is a IEEE Computer Society's Golden Core Member and is Doctor Honoris Causa of the Technical University of Budapest.

Mohammad Ibrahim received the B.Sc. and Ph.D. degrees from the University of Newcastle Upon Tyne, UK, in 1982 and 1985, respectively.

From 1982 to 1985, he was an Oversees Research Student Award holder, and held a BT Short Term Fellowship during Summer, 1986. He is currently a Professor of Computer Engineering at King Fahd University (KFUPM), and also holds a Visiting Professorship with the Department of Computer Science, Queens University Belfast, U.K. Prior to joining KFUPM, he held academic positions at Nottingham University, University Park, U.K., and DeMontfort University, where he was Professor and Head of the DSP Systems Group. His research interests include computer arithmetic, signal and image processing, cryptosystems, and application specific processors. He has more than 110 technical publications in journals and conferences.

Dr. Ibrahim is a Member of two technical committees of the IEEE Circuits and Systems Society, VLSI Systems and Applications, and Multimedia Systems and Applications. He also served on the IEEE Signal Processing Society Technical Committee on Design and Implementation of Signal Processing Systems. He currently serves on the Editorial Board of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, and the J*ournal of VLSI Signal Processing Systems*. He was a Member of the IEE Professional Group on Signal Processing, and is the past Chairman of the IEEE UK&RI Signal Processing Chapter. He has also served on the Technical Committees of several International Conferences, and he was the Chairman of the first IEEE Signal Processing Systems Workshop in 1997. He is the Coguest Editor of three special issues in the *Journal of VLSI Signal Processing Systems*.

Yehea Ismail was born in Giza, Egypt, on November 11, 1971. He received the B.Sc. (Hons.) and M.S. degree in electronics, with distinction, from Cairo University, Egypt, in 1993 and 1996, and the M.S. and Ph.D. degrees from the University of Rochester, Rochester, NY, in 1998 and 2000, respectively.

He is currently an Assistant Professor with Northwestern University, Evanston, IL. He was with IBM Cairo Scientific Center (CSC) from 1993 to 1996, and with IBM Microelectronics from 1997 to 1999. He has coauthored more than 47 technical papers and a book. His primary research's interests include interconnect, noise, innovative circuit simulation, and related circuit level issues in high performance VLSI circuits.

Dr. Ismail is on the Editorial Boards of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I. FUNDAMENTAL THEORY AND APPLICATIONS, and is a Guest Editor for a Special Issue of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS on "On-Chip Inductance in High Speed Integrated Circuits." He is also the Technical Chair for the International Workshop on System-on-Chip. He was selected as the 2002 IEEE Circuits and Systems Society's Outstanding Young Author Award Winner and won the 2002 National Science Foundation Career Award. He was also awarded the Best Teacher Award from Northwestern University in 2003.

Niraj K. Jha (S'85–M'85–SM'93–F'98) received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, in 1981, the M.S. degree in electrical engineering from SUNY at Stony Brook, NY, in 1982, and the Ph.D. degree in electrical engineering from the University of Illinois, Urbana-Champaign, in 1985.

He is currently a Professor of Electrical Engineering at Princeton University, NJ. He is also the Director of the Center for Embedded System-on-a-chip Design funded by New Jersey Commission on Science and Technology. He has coauthored three books *Testing and Reliable Design of CMOS Circuits* (Norwell, MA: Kluwer, 1990), *High-Level Power Analysis and Optimization* (Norwell, MA: Kluwer, 1998), and *Testing of Digital Systems* (Cambridge, U.K.: Cambridge Univ. Press, 2003). He has also authored three book chapters, has authored or coauthored more than 230 technical papers, and has received 11 U.S. patents. His research interests include low-power hardware and software design, computer-aided design of integrated circuits and systems, digital system testing, and distributed computing.

He has served as an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING. He is currently serving as an Editor of IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, *Journal of Electronic Testing: Theory and Applications* (JETTA), and the *Journal of Embedded Computing*. He has served as the Guest Editor for the JETTA Special Issue on high-level test synthesis, and has also served as the Program Chairman of the 1992 Workshop on Fault-Tolerant Parallel and Distributed Systems. He is the recipient of the AT&T Foundation Award, the NEC Preceptorship Award for Research Excellence, and the NCR Award for Teaching Excellence. He has coauthored six papers which have won the Best Paper Award at ICCD'93, FTCS'97, ICVLSID'98, Design Automation Conference (DAC) 1999, PDCS'02, and ICVLSID'03. He is also coauthor of a paper selected for "The Best of International Conference on Computer-Aided Design (ICCAD): A collection of the best IEEE International Conference on Computer-Aided Design papers of the past 20 years."

Lizy Kurian John received the Bachelor's degree in electronics and telecommunication from the University of Kerala, India, the Master's degree in computer engineering, from the University of Texas, El Paso, and the Ph.D. degree in computer engineering from The Pennsylvania State University, University Park, in 1993.

In 1996, she joined the Electrical and Computer Engineering Department, University of Texas (UT), Austin, where she is currently an Associate Professor and is also a UT Austin Engineering Foundation Centennial Teaching Fellow. Prior to joining UT Austin, she was a Faculty Member with the University of South Florida, Tampa. Her research interests include high-performance processor and memory architectures, low-power design, reconfigurable architectures, rapid prototyping, field-Programmable gate-arrays, workload characterization, etc. She has published papers in the IEEE TRANSACTIONS ON COMPUTERS, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, ACM/IEEE International Symposium on Computer Architecture (ISCA), IEEE Micro Symposium (MICRO), IEEE High Performance Computer Architecture Symposium (HPCA), ACM International Symposium on Low-Power Electronics and Design (ISLPED), etc., and has a U.S. patent for a field programmable memory cell array chip. Her research has been supported by the National Science Foundation, the State of Texas Advanced Technology program, DARPA, IBM, Intel, Motorola, DELL, AMD and Microsoft Corporations. She is a recipient of National Science Foundation CAREER Award, Junior Faculty Enhancement Award from Oak Ridge Associated Universities, IBM Austin Center for Advanced Studies (CAS) Fellowship, UT Austin Engineering Foundation Faculty Award (2001), and the Halliburton, Brown, and Root Engineering Foundation Young Faculty Award in 1999. She is a Member of the IEEE Computer Society, ACM, and ACM SIGARCH. She is also a Member of Eta Kappa Nu, Tau Beta Pi, and Phi Kappa Phi.

Andrew B. Kahng was born in 1963, in San Diego, CA. He received the A.B. degree in applied mathematics (physics) from Harvard University, Cambridge, MA, and the M.S. and Ph.D. degrees in computer science from the University of California at San Diego.

From June 1983 to June 1986, he was affiliated with Burroughs Corporation Micro Components Group in San Diego, where he worked in device physics, circuit simulation, and CAD for VLSI layout. In July 1989, he joined the Computer Science Department, University of California, Los Angeles (CLA) as an Assistant Professor, became Associate Pprofessor in July 1994, and a Professor on July 1998. From April 1996 to September 1997, he was on sabbatical leave and leave of absence from UCLA, as a Visiting Scientist at Cadence Design Systems, Inc. He resumed his duties at UCLA in Fall 1997, and presently serves as the Vice Chair for the Computer Science Department's Graduate Studies Program. His research interests include VLSI physical layout design and performance analysis, combinatorial and graph algorithms, stochastic global optimization, and the optimization foundations of computational commerce.

Professor Kahng has received the National Science Foundation Research Initiation and Young Investigator Awards, six Best Paper nominations and a Design Automation Conference (DAC) Best Paper Award. He was the Founding General Chair of the 1997 ACM/IEEE International Symposium on Physical Design, Cofounder of the ACM Workshop on System-Level Interconnect Prediction, and defined the physical design roadmap as a Member of the Design Tools and Test technical working group for the 1997, 1998, and 1999 renewals of the SIA Technology Roadmap for Semiconductors. He has also served as a Member of the EDA Council's EDA 200X task force.

Israel Koren (S'72–M'75–SM'87–F'91) received the B.Sc., M.Sc. and D.Sc. degrees, in electrical engineering, from the Technion—Israel Institute of Technology, Haifa, in 1967, 1970, and 1975, respectively.

He is currently a Professor with the Department of Electrical and Computer Engineering, University of Massachusetts, Amherst. Previously, he held positions with the Technion—Israel Institute of Technology, the University of California at Berkeley, the University of Southern California, Los Angeles, and the University of California, Santa Barbara. He has been a Consultant to several companies including Analog Devices, AMD, Digital Equipment Corp., IBM, Intel, National Semiconductor and Tolerant Systems. He was editor and coauthored of, *Defect and Fault-Tolerance in VLSI Systems, Vol. 1*, (New York: Plenum, 1989), and is author of the textbook *Computer Arithmetic Algorithms, 2nd Edition*, (Natick, MA: A. K. Peters, 2002). His current research interests include Models for Yield of VLSI circuits, Techniques for Yield and Reliability Enhancement, Fault-Tolerant Architectures, Real-time systems and Computer Arithmetic.

Dr. Koren has been a Guest Editor for the IEEE TRANSACTIONS ON COMPUTERS, the special issue on *Computer Arithmetic*, July 2000, and the special issue on *High Yield VLSI Systems*, April 1989, and served on the Editorial Board of these Transactions from 1992 to 1997. He has also served as General Chair, Program Chair, and Program Committee Member for numerous conferences.

Radu Marculescu (M'94) received the Ph.D. degree from the University of Southern California, Los Angeles, in 1998.

In 2000, he joined the Faculty of the Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA, where he is currently an Assistant Professor. He and his group perform research on formal methods for SOC design of embedded applications. Of particular interest are fast methods for power and performance analysis that can guide the design process of portable information devices. Currently, the group develops novel approaches for exploiting concurrency and communication aspects in the design and optimization of complex heterogeneous applications. His research interests include System-on-Chip design methodologies, NOC's and fault-tolerant communication, and ambient intelligent systems.

Dr. Marculescu was awarded the National Science Foundation's Career Award for the System-Level Power/Performance Analysis for Embedded Systems Design in 2001. He recently received three Best Paper Awards in the area of systems design methodologies in the 2001 and 2003 editions of the Design and Test Conference in Europe (DATE), and the 2003 edition of the Asia and South Pacific Design Automation Conference (ASP-DAC). He was also awarded the 2002 Ladd Research Award from Carnegie Institute of Technology.

Vijaykrishnan Narayanan received the B.E degree in computer science and engineering from SVCE, University of Madras, India, in 1993 and the Ph.D. degree in computer science and engineering from the University of South Florida, Tampa, in 1998.

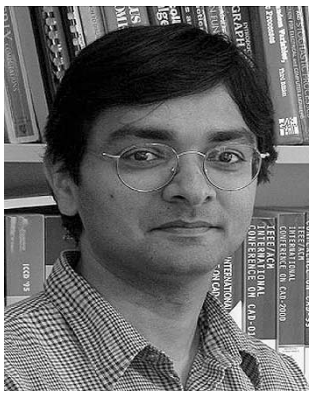
In 1998, he joined the Department of Computer Science and Engineering, Pennsylvania State University, University Park, where he is currently an Associate Professor. His research interests include energy-aware reliable systems embedded Java, nano/VLSI systems, and computer architecture. He has authored or coauthored more than 100 papers in these areas. His current research projects are supported by National Science Foundation, DARPA/MARCO Gigascale Silicon Research Center, Office of Naval Research, Semiconductor Research Consortium and Pittsburgh Digital Greenhouse.

Dr. Narayanan served as General Chair for the IEEE Computer Society Annual Symposium on VLSI in 2003 and as the treasurer for the International Symposium on Low-Power Electronics and Design since 2001. He also serves as the Vice-Chair for Student Activities for the IEEE Computer Society. He has received several awards including the IEEE CAS VLSI Transactions Best Paper Award in 2002, the Penn State CSE Faculty Teaching Award in 2002, the ACM SIGDA Outstanding New Faculty Award in 2000, Upsilon Pi Epsilon Award for academic excellence in 1997, the IEEE Computer Society Richard E. Merwin Award in 1996, and the University of Madras First Rank in Computer Science and Engineering in 1993.

Steven M. Nowick received the B.A. degree from Yale University, New Haven, CT., and the Ph.D. degree in computer science from Stanford University, Palo Alto, CA, in 1993.

He is currrently an Associate Professor of Computer Science and Electrical Engineering at Columbia University, NY. His general research interests include asynchronous circuits, computer-aided digital design, low-power and high-performance digital systems, and logic synthesis. His recent research focus has been mainly on asynchronous digital design (CAD tools, high-speed pipelines, applications) and mixed-timing systems.

Dr. Nowick received an National Science Foundation (NSF) Faculty Early Career (CAREER) Award in 1995, an Alfred P. Sloan Research Fellowship also in 1995, and an NSF Research Initiation Award (RIA), in 1993. He received Best Paper Awards at the IEEE 1991 International Conference on Computer Design and at the IEEE Async-2000 Symposium, and was a Best Paper Finalist at Async-98, Async-02, and Async-03. He was a cofounder of the IEEE Async Symposia series, and served as its Program Cochair in 1994 and 1999. He was also the Program Chair of the 2002 IEEE/ACM International Workshop on Logic and Synthesis (IWLS). He has been a Member of a number of international program committees, including Design Automation Conference (DAC), International Conference on Computer-Aided Design (ICCAD), DATE, Async, ICCD, TAU, IWLS and VLSI Design. He was also a Guest Editor of a special issue of PROCEEDINGS OF THE IEEE" on Asynchronous Design, February 1999, and he was Guest Coeditor of a Special Section of IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN, June 2003, devoted to some top papers from the IWLS-02 workshop. He has been an Associate Editor for TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS since 2001.



Sachin Sapatnekar (S'86–M'88–SM'99) received the B.Tech. degree from the Indian Institute of Technology, Bombay in 1987, the M.S. degree from Syracuse University, NY, in 1989, and the Ph.D. degree from the University of Illinois at Urbana-Champaign, in 1992.

From 1992 to 1997, he was an Assistant Professor with the Department of Electrical and Computer Engineering, Iowa State University, Ames. He is currently a Professor in the Department of Electrical and Computer Engineering at the University of Minnesota, Minneapolis. He has coauthored two books, *Timing Analysis and Optimization of Sequential Circuits* and *Design Automation for Timing-Driven Layout Synthesis* (Norwell, MA: Kluwer), and is a Coeditor of a volume, *Layout Optimizations in VLSI Designs* (Norwell, MA: Kluwer). He has held positions on the Editorial Board of the IEEE TRANSACTIONS ON VERY LARGE INTEGRATION SYSTEMS, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—Part II: ANALOG AND DIGITAL SIGNAL PROCESSING, and has been a Guest Editor for two issues of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN. He has served on the Technical Program Committee for various conferences, and as Technical Program and General Chair for the Tau workshop and for the International Symposium on Physical Design. He is currently a Distinguished Visitor for the IEEE Computer Society and has been a Distinguished Lecturer for the IEEE Circuits and Systems Society. He is a recipient of the National Science Foundation Career Award and best paper awards at Design Automation Conference (DAC) 1997, ICCD 1998, DAC 2001, and DAC 2003.

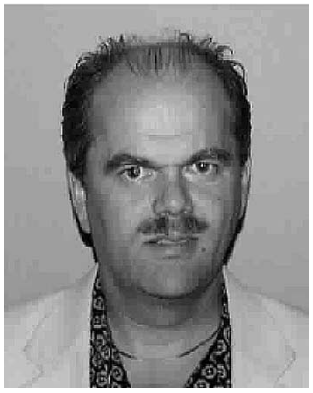
Majid Sarrafzadeh (S'82–M'82–SM'91–F'96) received the B.S., M.S., and Ph.D. degrees, in electrical and computer engineering, from the University of Illinois at Urbana-Champaign in 1982, 1984, and 1987, respectively.

In 1987, he became an Assistant Professor with Northwestern University, Evanston, IL. In 2000, he joined the Computer Science Department, University of California at Los Angeles (UCLA). His recent research interests include embedded and reconfigurable computing, VLSI computer-aided design, and the design and analysis of algorithms. He has published approximately 250 papers. He is a coeditor of *Algorithmic Aspects of VLSI Layout*" (Singapore: World Scientific, 1994), and coauthor of *An Introduction to VLSI Physical Design*" (New York: McGraw-Hill, 1996). He has collaborated with many industries in the past fifteen years including IBM and Motorola and many CAD industries and was the architect of the physical design subsystem of Monterey Design Systems main product. He is a cofounder of Hier Design, Inc., Santa Clara, CA.

Dr. Sarrafzadeh received a National Science Foundation Engineering Initiation Award, two Distinguished Paper Awards at the International Conference on Computer-Aided Design (ICCAD), and the Best Paper Award at the Design Automation Conference (DAC). He has served on the Technical Program Committee of numerous conferences in the area of VLSI Design and Computer-Aided Design (CAD), including ICCAD, DAC, EDAC, International Symposium on Physical Design (ISPD), field programmable gate arrays (FPGA), and DesignCon. He has served as Committee Chair of a number of these conferences. He is on the Executive Committee or Steering Committee of several conferences such as ICCAD, International Symposium on International Design (ISPD), and International Symposium on Quality Electronic Design (ISQED). He is the Program Committee Chair of ICCAD 2004. He is an Associate Editor of *ACM Transaction on Design Automation* (TODAES), and of IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN (TCAD).

Raghu Sastry (S'81–M'93–SM'99) received the B.E. (Hons.) degree in electronics engineering from the University of Madras, India, the M.S. degree in electrical engineering from the Indian Institute of Technology, Madras, and the Ph.D. degree in computer science and engineering from the University of South Florida, Tampa.

From 1985 to 1990, he was a Member of the Research Staff at the Indian Institute of Technology, Madras. From 1994 to 2000, he was with HAL Computer Systems, Campbell, CA, as a VLSI Design Manager for their Synfinity line of interconnect products. From 2000 to 2002, he was the Director of Product Development at RedSwitch Inc., Milpitas, CA, with a focus on custom and Rapid IO based interconnect solutions. Since 2003, he has been with Agilent Technologies Inc., Milpitas, CA, as a Director of Research and Development for storage, telecom, and server interconnect solutions. His research interests include parallel architectures, pattern matching, VLSI algorithms and architectures, high-performance switch design, high-speed signal transmission techniques, and all aspects of VLSI design. He has more than 20 publications in international journals and conference proceedings, and has been awarded seven U.S. patents.



Radu M. Secareanu (S'98–M'00) received the M.S. degree from the Polytechnic University of Bucharest, Romania, in 1990, and the M.S. and Ph.D. degrees, all in electrical engineering, from the University of Rochester, NY, in 1998 and 2000, respectively.

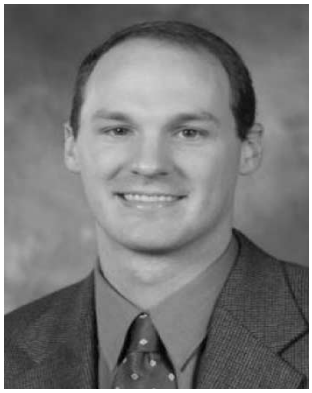
From 1990 to 1995, he was with IPRS Semiconductor, Bucharest, Romania, where he held various positions, primarily in research and development, working on a variety of circuit design issues. From 1996 to 2000, he was a Teaching and Research Assistant at the University of Rochester, while completing the Ph.D. degree on high performance IC design and on-chip noise immunity. During this time, he worked closely with Xerox Corporation in developing his research results. In 2000, he joined Motorola, Inc., Semiconductor Products Sector, Digital DNA(TM) Laboratories, in Tempe, AZ, working on multiple analog/RF and digital IC design challenges with close implications on present and future devices, circuits, and systems. Since 2002, he has been an Adjunct Professor in the Department of Electrical Engineering, Arizona State University, Tempe. He has authored many papers and three issued patents (others pending) in the fields of high-performance IC design and related noise immunity aspects. His current research interests include the areas of high-performance analog, mixed-signal and digital VLSI IC design, and signal integrity, with close implications on future technologies and applications.

Dr. Secareanu has served on several committees and boards.

Sunil D. Sherlekar (M'98) received the B.Tech. (EE), M.Tech. (CSE), and Ph.D. degrees from the Indian Institute of Technology (IIT) Bombay, Mumbai, India.

From 1982 to 1992, he was on the Faculty of the Department of Computer Science and Engineering at IIT, Bombay. From 1992 to 2002, he was with Sasken Communication Technologies, Bangalore, India, as Chief Technology Officer. Since 2002, he has been with Tata Consultancy Services as Head of their Center of Excellence for Embedded Systems. He is also an Adjunct Professor with the Department of Electrical Engineering, IIT Bombay. His research interests include VLSI Design and Testing, EDA, hardware description languages, and optimal implementation of signal processing. He has published several papers in these areas and also a book (published by Kluwer Academic).

Dr. Sherlekar has been Program Chair and General Chair for several IEEE sponsored conferences as well as other conferences. He is on the Steering Committee of the Asia and South Pacific Design Automation Conference. He is also on the Editorial Board of *Journal of Testing: Theory and Applications*, published by Kluwer Academic, Singapore.



Dennis Sylvester (SM'95–M'00) received the B.S. degree in electrical engineering *summa cum laude*, from the University of Michigan, Ann Arbor, in 1995, and the M.S. and Ph.D. degrees in electrical engineering from University of California (UC), Berkeley, in 1997 and 1999, respectively.

From 1996 to 1998, he was with Hewlett-Packard Laboratories, Palo Alto, CA. He was a Senior Research and Development Engineer with the Advanced Technology Group of Synopsys, Mountain View, CA, and is currently an Assistant Professor of Electrical Engineering at the University of Michigan, Ann Arbor. He has published numerous papers in his field of research, which includes the modeling, characterization, and analysis of on-chip interconnects low-power circuit design and design automation techniques, and variability-aware circuit approaches.

Dr. Sylvester received a National Science Foundation Career Award, the 2000 Beatrice Winner Award at ISSCC, two Outstanding Research Presentation Awards from the Semiconductor Research Corporation, and a Best Student Paper Award at the 1997 International Semiconductor Device Research Symposium. His doctoral dissertation was recognized with the 2000 David J. Sakrison Memorial Prize as the most outstanding research in the U.C. Berkeley Electrical Engineering and Computer Science Department. He is the recipient of the 2003 ACM SIGDA Outstanding New Faculty Award and also the 2003 Ruth and Joel Spira Outstanding Teaching Award in the Michigan College of Engineering. He is on the Technical Program Committee of several design automation and circuit design conferences and served as General Cochair for the 2003 ACM/IEEE System-Level Interconnect Prediction (SLIP) Workshop. In addition, he helps to define the circuit and physical design roadmap as a Member of the International Technology Roadmap for Semiconductors (ITRS) U.S. Design Technology Working Group. He is a Member of ACM, American Society of Engineering Education, and Eta Kappa Nu.

Ranga Vemuri (S'87–M'88–SM'00) received the M.Tech. degree from the Indian Institute of Technology at Kharagpur in 1985, and the Ph.D. degree from Case Western Reserve University, Cleveland, OH, in 1988.

He is a Professor in the Department of Electrical and Computer Engineering and Computer Science and the Director of the Laboratory for Digital Design Environments at the University of Cincinnati, OH. His research interests include the computer-aided design of VLSI systems, reconfigurable computers, mixed signal design automation, formal verification, high-level synthesis, and hardware description languages. He has coauthored about 130 research publications in these areas and graduated over 20 Ph.D. students and 30 M.S. students. His research has been sponsored by the Defense Advanced Research Projects Agency, US Air Force Research Laboratory, the National Science Foundation, the Semiconductor Research Corporation, the State of Ohio and several industries.

Dr. Vemuri is the recipient of the University of Cincinnati Faculty Achievement Award, the Sigma Xi Outstanding Young Researcher Award, the William Middendorf Distinguished Research Award, the William Restemeyer Distinguished Teaching Award, the Engineering Tribunal Award for Outstanding Teaching, and several Best Paper awards at various international conferences including VLSI Design in 2000, FPL in 1999, and the International Conference on Computer Design (ICCD) in 1998. He was a Guest Editor of the IEEE Computers Special Issue on Reconfigurable Computers: Technology and Applications and of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS Special Issue on Adaptive and Reconfigurable VLSI Systems.

An-Yeu (Andy) Wu (S'91–M'96) received the B.S. degree from National Taiwan University, Taipei, R.O.C., in 1987, and the M.S. and Ph.D. degrees in electrical engineering, from the University of Maryland, College Park, in 1992 and 1995, respectively.

From 1987 to 1989, he served as a Signal Officer in the Army, Taipei, Taiwan, for his mandatory military service. From 1990 to 1995, he was a Graduate Teaching and Research Assistant with the Department of Electrical Engineering and Institute for Systems Research at the University of Maryland, College Park. From August 1995 to July 1996, he was a Member of the Technical Staff at AT&T Bell Laboratories, Murray Hill, NJ, where he worked on high-speed transmission IC designs. From 1996 to July 2000, he was with the Electrical Engineering Department, National Central University, Taiwan. He is currently an Associate Professor with the Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taiwan. His research interests include low-power/high-performance VLSI architectures for digital-signal processing (DSP) and communication applications, adaptive/multirate signal processing, and reconfigurable broadband access systems and architectures.

Dr. Wu is currently serving as an Associate Editor for *Eurasip Journal of Applied Signal Processing*, and is a Guest Editor for a Special Issue on Signal Processing for Broadband Access Systems: Techniques and Implementations. He has served on the Technical Program Committees of the International Conference on Image Processing (ICIP), IEEE Workshop on Signal Processing Systems (SiPS), IEEE Asia-Pacific Conference on ASICs (AP-ASIC), IEEE International Symposium on Circuits and Systems (ISCAS), IEEE International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), IEEE International Conference on Multimedia and Expo (ICME), and IEEE International SOC Conference.

Chung-Yu Wu (S'76–M'76–SM'96–F'98) was born in Chiayi, Taiwan, R.O.C. He received the M.S. and Ph.D. degrees in electronics engineering, from the National Chiao-Tung University, Taiwan, R.O.C., in 1976 and 1980, respectively.

From 1980 to 1984, he was an Associate Professor with the National Chiao-Tung University. From 1984 to 1986, he was a Visiting Associate Professor with the Department of Electrical Engineering, Portland State University, OR. Since 1987, he has been a Professor with National Chiao-Tung University. From 1991 to 1995, he was rotated to serve as Director of the Division of Engineering and Applied Science in the National Science Council. Currently, he is the Centennial Honorary Chair Professor at the National Chiao-Tung University. He has published more than 69 journal papers and 92 conference papers on several topics, including digital integrated circuits, analog integrated circuits, computer-aided design, neural networks, ESD protection circuits, special semiconductor devices, and process technologies. He also has 17 patents including nine U.S. patents. His current research interests include low-voltage low-power mixed-mode integrated circuit design, hardware implementation of visual and auditory neural systems, and RF integrated circuit design.

He was Awarded the Outstanding Research Award by the National Science Council in 1989 and 1995, and the Outstanding Engineering Professor by the Chinese Engineer Association in 1996.

Michael Pham received the B.S degree in chemistry from San Diego State University, San Diego, CA, in 1995, and the B.S degree in computer science from University of South Florida, Tampa, in 2003.

He is currently serving as the Editorial Administrative Assistant for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.