Guest Editorial
Special Section on Configurable Computing Design—II: Hardware Level Reconfiguration

THE SECOND issue "Hardware Level Reconfiguration" of the Special Section on Configurable Computing Design deals with hardware level problems: how to build efficient gate arrays; security and fault tolerance issues on configurable hardware; and implementing floating-point arithmetic and specific decoders on field-programmable gate arrays (FPGAs).

The first two papers of this issue deal with gate level problems: with efficient building of reconfigurable logic arrays. The first paper, "A Low-Power Reconfigurable Logic Array Based on Double Gate Transistors," by P. Beckett, presents a new logic array technology on a gate level. Contrasting with current FPGA structures in which logic and interconnect are built and configured separately, in the new array technology each cell can act as logic or interconnect, or both. This is achieved by using double gate transistors technology.

In "Stochastic Physical Synthesis Considering Prerouting Interconnect Uncertainty and Process Variation for FPGAs," Y. Lin *et al.* present the in-depth study on stochastic physical synthesis algorithms leveraging statistical static timing analysis for FPGAs. Process variation and prerouting interconnect delay uncertainty affect timing and power for VLSI designs. The stochastic clustering, placement, and routing reduce the yield loss. The majority of improvements are achieved during clustering and placement. The paper studies the interaction between each individual design stage and demonstrates that an effective and efficient flow can be developed to use stochastic clustering and deterministic placement and routing.

The next three papers deal with fault tolerance management, security, and intrusion detection in reconfigurable computing environment. The first paper of this group, "Applying Dynamic Reconfiguration for Fault Tolerance in Fine-Grained Logic Arrays," by P. Zipf, deals with the realization of a fault tolerance technique which consists of three parts: fault detection, fault reconfiguration, and fault recovery. All these parts are implemented completely in hardware and form a self-contained system. The technique discussed can be used to exploit dynamic reconfiguration capabilities of programmable arrays to alleviate system vulnerability and thus to enhance their overall reliability.

The paper "Reconfigurable Hardware for High-Security/High-Performance Embedded Systems: The SAFES Perspective," by G. Guy *et al.*, proposes the security architecture for embedded systems (SAFES). The SAFES architecture is based on three main ideas: 1) reconfigurable security primitives; 2) reconfigurable hardware monitors; and 3) a hierarchy of security controllers at the primitive, system, and executive level. This paper stresses that reconfigurable hardware is a real solution to provide high-security/high-performance systems.

In the last paper of this group, "Scalable Multigigabit Pattern Matching for Packet Inspection" by I. Sourdis *et al.*, hardware-based scanning and analyzing packets payload in order to detect hazardous contents are presented. The paper presents two pattern matching techniques to compare incoming packets against intrusion detection search patterns. Both approaches are evaluated in terms of performance and area cost. Proposed designs achieve at least 30% higher efficiency compared to previous work, measured in throughput per area required per search character.

The next two papers consider implementation of floating-point arithmetic operations on configurable computing platform.

In "Area-Efficient Arithmetic Expression Evaluation Using Deeply Pipelined Floating-Point Cores," R. Scrofano *et al.*, deal with high-performance floating-point arithmetic. To achieve high-performance floating-point cores must be deeply pipelined. The proposed designs effectively hide the pipeline latency of the floating-point cores. Experimental results show that the areas of these designs increase linearly with the number of types of operations in the expression and that the designs occupy less area and achieve higher throughput than designs generated by a commercial hardware compiler.

The paper "Architectural Modifications to Enhance the Floating-Point Performance of FPGAs," by M. J. Beauchamp *et al.*, considers three architectural modifications that make floating-point operations more efficient on FPGAs. The first modification embeds floating-point multiply–add units in an island-style FPGA. The next two modifications use variable length shifters: 1) a coarse-grained approach, where variable length shifters are embedded in the FPGA fabric and 2) a fine-grained approach, where a 4:1 multiplexer unit is added inside the slices, in parallel to the 4-LUTs.

The last paper of this issue brings us back to the configurable architecture of complex application. The paper "System Architecture and Implementation of MIMO Sphere Decoders on FPGA," by X. Huang *et al.*, presents the architecture and implementations for two typical sphere decoding algorithms. Three levels of parallelism are explored to improve the decoding rate: the concurrent execution of the channel matrix preprocessing on embedded processor and the decoding function on the customized hardware modules, the parallel execution of real/imaginary parts decoding for complex constellations, and the concurrent execution of multiple states during the closest lattice point search.

We hope that these two Special Sections on Configurable Computing Design, covering high-level and hardware level reconfiguration techniques, will raise your awareness about the scope of reconfigurable or adaptive computing.

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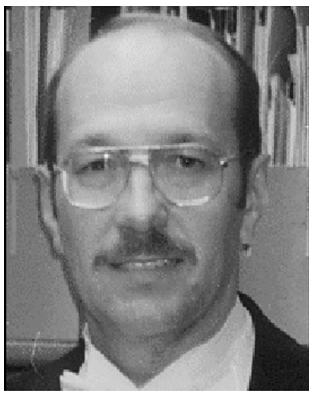

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He is the Managing Director and the founder of a newly established company, Conhard Design Ltd., London, U.K., in the area of mobile computing applications and hardware. He is also a Visiting Fellow of the Reading University, Reading, U.K., and the London South Bank University, London, U.K. His research interests include the design of high-performance application-specific processors, massively parallel computer systems, and reconfigurable architectures in mobile computing and multimedia applications. His main interests focus on the theory and design of regular processor arrays and mapping algorithms onto space and time, i.e., into hardware. Also, his interests include computer networking, mobile computing, and web-based technologies. He has published over 70 scientific papers including a monograph on a synthesis of regular processor arrays. He is the Founder and the Chairman of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA) in Las Vegas, NV, and the initiator of Mobile Computing Hardware Architecture (MOCHA) Symposium, HI. He is the Guest Editor of a series of special issues on designing dedicated processors on reconfigurable computing platform.

Dr. Plaks is a member of the New York Academy of Sciences and the U.K. Chapter of the Association for Computing Machinery Special Interest Group on Design Automation (ACM SIGDA). His biography is included in the Marquis *Who's Who in Science and Engineering*.