Guest Editorial: Special Section on Asynchronous Circuits and Systems

THE SPECIAL Section in this issue covers different aspects of asynchronous design. This is an area of increasing interest in the last few years triggered by the new challenges dictated by the continuous miniaturization of integrated circuits. Variability, power, noise, and electromagnetic interference are some of the aspects that designers have to face today to make their circuits efficient, robust and with affordable manufacturing costs. Imposing a rigid clock to a circuit that internally experiments significant variability is like keeping a sparrow in a cage. The delay margins to ensure correctness are increasing as device and interconnect variability dominate in the timing characterization of the components of the circuits. In addition, power consumption is often becoming the most severe limitation to achieve the performance requirements of the specification.

Asynchronous circuits, with their different forms of implementation, contribute to meliorate some of the features of circuits finding more favorable points in the power/performance/area design space. Some examples may help to illustrate these features.

Synchronization in asynchronous circuits is local, thus increasing the spatial correlation between the circuit delays and the synchronization signals, usually implemented as handshakes between local clocks. Hence, the margins to cover the potential variability can be significantly reduced and the performance of the circuit can be naturally adapted to the operating conditions determined by the environment (e.g., voltage and temperature). In some classes of circuits, such as delay-insensitive circuits, the immunity to variability is complete.

Asynchronous circuits also contribute to reduce dynamic power. The components of the circuit only work when some computation is needed and this can be implemented elegantly by simply associating computations with the handshake signals that indicate the availability of information.

Electromagnetic interference is another concerning aspect of synchronous circuits that concentrate their switching activity close to the clock edges. Asynchronous circuits spread this activity more evenly across the spectrum since the activity is determined by local handshakes that have a lower timing correlation.

This issue presents five regular papers and two short papers exposing recent advances in the design of asynchronous systems. Most of the contributions were originally presented at the *14th IEEE International Symposium on Asynchronous Circuits and Systems* that was held in Newcastle upon Tyne, U.K., in April 2008. Out of 23 submissions for this Special Section, the papers were selected after a thorough evaluation process.

The first paper, "Efficient Automatic Resolution of Encoding Conflicts Using STG Unfoldings" by Khomenko, proposes an efficient solution for state encoding in asynchronous controllers. This is a logic synthesis problem as important as state encoding for finite-state machines in sequential logic synthesis. The additional constraints required for asynchronous circuits make automation essential for this problem.

The second paper, "Soft-Error Tolerance and Mitigation in Asynchronous Burst-Mode Circuits" by Almukhaizim *et al.*, is concerned about the robustness of asynchronous controllers. It proposes two efficient techniques to increase the tolerance and mitigate the susceptibility to soft errors, which are predicted to increase with deep-submicron technologies.

The third paper, "Asynchronous Computing in Sense Amplifier-Based Pass Transistor Logic" by Liu *et al.*, presents a novel idea to implement low-energy asynchronous logic. The scheme uses sense amplifier-based pass transistor logic to efficiently do the computations and detect their completion.

The fourth paper, "Power Reduction of Asynchronous Logic Circuits Using Activity Detection" by Thonnart *et al.*, faces the problem of static power consumption and proposes an innovative approach to reduce the supply voltage. The approach is based on the detection of periods of inactivity to control the voltage regulator and power down the circuits in standby mode automatically.

The fifth paper, "Constrained Asynchronous Ring Structures for Robust Digital Oscillators" by Hamon *et al.*, proposes a new approach to design robust ring oscillators using asynchronous logic. By using a high-level ring model and accurate timing information, the authors design high-resolution ring structures that are robust to process variability.

This Special Section also includes two short papers addressing variability from different points of view. In the first paper, "Scalable Multi-Input–Multi-Output Queues with Application to Variation-Tolerant Architectures" by van Berkel and van Roermund, an innovative design for multi-input–multi-output asynchronous queues is proposed. These queues are suitable for fine-grain load balancing in variable-tolerant architectures. Finally, the last paper, "Asynchronous Protocol Converters for Two-Phase Delay-Insensitive Global Communication" by McLaughlin *et al.*, presents new schemes for the conversion between two- and four-phase protocols. These converters provide robust solutions for delay-insensitive global communications.

For those readers not familiar with the asynchronous technology, we suggest to them to gain some knowledge by reading some of the books, tutorials, or surveys that can easily be found in the literature. We then encourage them to judge by themselves the new opportunities offered by asynchronous circuits and the eligibility of this technology to solve the design problems faced in their work environments.

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Currently, he is a Professor with the Department of Software, Universitat Politecnica de Catalunya. In 1988, he was a visiting scholar at the University of California, Berkeley. He is a co-founder of Elastix Corp., a company using asynchronous technology for low-power circuits. His research interests include formal methods and computer-aided design of VLSI systems, with special emphasis on asynchronous circuits, concurrent systems, and logic synthesis. He has coauthored numerous research papers and has been invited to present tutorials at various conferences. He has served on the technical committees of several international conferences in the field of design automation and concurrent systems.

Dr. Cortadella was a recipient of the Best Paper Awards at the International Symposium on Advanced Research in Asynchronous Circuits and Systems and at the Design Automation Conference, both in 2004. In 2003, he was the recipient of a Distinction for the Promotion of the University Research by the Generalitat de Catalunya.

Alexander Taubin (SM'96) received the M.Sc. and Ph.D. degrees in computer science and engineering from Electrotechnical University of St. Petersburg, St. Petersburg, Russia.

In 2002, he joined Electrical and Computer Engineering Department of Boston University as Associate Professor. From 1979 to 1989, he was a Research Fellow with the Computer Department, St. Petersburg Mathematical Economics Institute, USSR Academy of Science. From 1988 to 1993, he was a Senior Researcher with the R&D Coop. TRASSA. From 1991 to 1992, he was also a Postdoctoral Researcher with the Department of Advanced Research, Institute of Microelectronics, Zelenograd, Russia. From 1993 to 1999, he was a Professor with the Department of Computer Hardware, University of Aizu, Japan. In 1999, he joined Theseus Logic, Inc. Sunnyvale, CA, as a Senior Scientist. His current research interests include design and design automation of asynchronous pipelined systems, high secure, high speed and low power devices and systems. He coauthored three books in asynchronous design and has published more than 60 journal and conference papers.

Dr. Taubin was a recipient of the Best Paper Award from the 11th Design, Automation, and Test in Europe (DATE 2008) Conference. He has served on the technical committees of several international conferences in his field. He was Program Cochair of the 14th International Symposium on Advanced Research in Asynchronous Circuits and Systems (Async2008) and the 2nd International Symposium on Advanced Research in Asynchronous Circuits and Systems (Async1996).