Guest Editorial

COMPUTER systems have evolved at tremendous speed and have today conquered a great variety of ecologic spaces and niches from supercomputers to tiny sensor nodes.

Just as diverse as the applications, are the requirements. Size, form factor, performance, bandwidth, power consumption, cost, fault tolerance, and security issues are among the common requirements imposed on many computing systems. Fortunately, technology has evolved to provide a broad spectrum of potential solutions for all the specific applications. However, it takes time to find a reasonably good solution out of the myriad possible. As the design space quickly grows and is also increasingly constrained by diverse requirements and demands, design tools and methodologies are hard pressed to keep up the pace with the promises of technology on one hand, and the demands of applications on the other.

As a consequence of these developments, design technology has become highly sophisticated as well as diverse. From the focus on minimizing hardware area and maximizing operations per second in the early beginnings of this discipline, the objectives have both shifted and become much broader and nuanced. Power consumption has matched and even overshadowed both area and performance as the most dominating concern because both cost and end user performance are often limited by the capacity of the power delivery and the heat dissipation system. This is noticeably illustrated by this special section. Most articles declare power and energy consumption as one of their major concerns and several have it as their main theme. Other important trends of the field that are manifest in the present special section, include the increased focus on communication, configurability, customization, and software.

This Special Section had as its starting point the International Conference on Hardware/Software Codesign and System Synthesis, in September 2004 in Stockholm, Sweden. However, all the researchers in the community were encouraged to submit their work, regardless if it has been presented at the conference or not. The response was overwhelming. Sixty-one manuscripts had been submitted, many of which were of very high quality. The review process proved challenging and time consuming.

Given the number and quality of submissions, the Editor-in-Chief has kindly offered to allow this Special Section to extend over two consecutive issues. Therefore, we were able to accept in total 15 papers out of the 61 submissions. The first part contains eight papers.

The paper "Parallel programming models for a multiprocessor SoC platform applied to networking and multimedia" by P. G. Paulin, C. Pilkington, M. Langevin, E. Bensoudane, D. Lyonnard, O. Benny, B. Lavigueur, D. Lo, G. Beltrame, V. Gagné, and G. Nicolescu addresses the challenging question of how to program today's and tomorrow's highly complex, heterogeneous multicore SoCs. It proposes a homogeneous programming model for heterogeneous platforms that offers both message passing and shared-memory-based communication.

Three papers concentrate on the communication bottleneck by analyzing or optimizing the communication architecture. In "Efficient exploration of bus-based system-on-chip architectures" by S. Kim and S. Ha, the authors describe a technique to optimize a bus-based communication architecture for a well-understood application based on a communication and memory access trace.

U. Y. Ogras and R. Marculescu also optimize the communication architecture which they assume is a packet switched communication network. In "It's a small world after all: NoC performance optimization via long-range link insertion," the authors customize a regular communication mesh by inserting long links across several tiles in the mesh, and report a bandwidth increase around 50% for industrial benchmark applications.

The paper "Modeling operation and microarchitecture concurrency for communication architectures with application to retargetable simulation" by X. Zhu, W. Qin, and S. Malik, presents a simulation framework based on a formal concurrency model. It allows to generate application-specific simulators for efficient and accurate analysis of on-chip message passing-based communication performance at an early design stage.

The following three papers focus on energy awareness and low-power consumption.

"Energy minimization for real-time systems with (m, k)-guarantee" by L. Niu and G. Quan, combines the objective to minimize power consumption with the provision of quality of service for soft real-time systems. It proposes a scheduling method that guarantees that m-out-of-k jobs meet their deadline while the total energy consumption is minimized.

The paper "System-level power-performance tradeoffs for reconfigurable computing" by J. Noguera and R. M. Badia, explores power-performance tradeoffs for streaming applications mapped on field-programmable gate arrays (FPGAs). They conclude that, in order to minimize power, it is usually more beneficial to use an efficient, static HW/SW partitioning algorithm while dynamic reconfiguration may be preferable for maximizing performance.

Rather than optimizing for low-power consumption, the paper "A table masking countermeasure for low-energy secure embedded systems" by C. H. Gebotys, proposes a method to protect sensitive information such as cryptographic keys in low-power embedded devices from differential power analysis and differential electromagnetic analysis. The protection mechanism is based on a table-masking technique which provides random masking with very low energy overhead to make it suitable for low-power mobile devices.

Finally, the last paper of this special section which is printed in this, "ISEGEN: An iterative-improvement-based ISE generation technique for fast customization of processors" by P. Biswas, S. Banerjee, N. D. Dutt, L. Pozzi, and P. Ienne, de-

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scribes the customization of processor architectures by means of instruction set extensions with the goal to increase the performance for a given application. The proposed algorithm is based on an iterative hardware/software partitioning algorithm at the granularity level of individual instructions.

We sincerely hope that the snapshot of cutting edge research in the field of hardware/software codesign and system synthesis that this and the next month's issues present, is of interest to you and that you enjoy reading it.

We would like to express our gratitude to the many reviewers who very carefully and professionally screened all the submissions, and through their insightful comments and suggestions ensured the very high quality of the papers. We would also like to thank all the authors for their great efforts and we regret that we could not accept more of the excellent articles submitted to this Special Section. Finally, we would like to thank the Editor-in-Chief, Professor Nagarajan Ranganathan, for generously providing the space for two special sections, and we acknowledge with gratitude the excellent support and cooperation by him and Michael Pham at the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS office.

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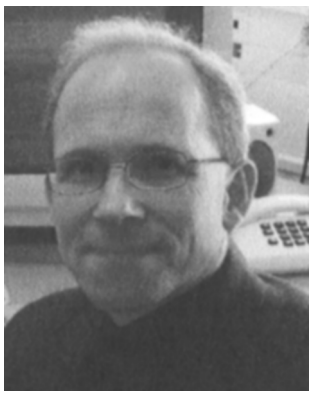

Petru Eles (M'99) received the Ph.D. degree in computer science from the Politehnica University of Bucharest, Bucharest, Romania, in 1993.

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Dr. Eles is an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, and of the *IEE Proceedings—Computers and Digital Techniques*. He has served as a Program Committee member for numerous international conferences in the areas of Design Automation, Embedded Systems, and Real-Time Systems, and as a TPC co-chair and general co-chair of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis. He has served as an IEEE CAS Distinguished Lecturer for 2004 and 2005. He was a corecipient of the Best Paper Awards at the European Design Automation Conference in 1992 and 1994, and at the Design Automation and Test in Europe Conference in 2005, and of the Best Presentation Award at the 2003 IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis. He is a member of ACM.

Axel Jantsch (M'96) received the Dipl.Ing. and the Dr.Tech. degrees from the Technical University Vienna, Vienna, Austria, in 1988 and 1992, respectively.

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Dr. Jantsch has served on a number of technical program committees of international conferences such as FDL, DATE, CODES+ISSS, SOC, and HDLCON, and others. He has been the TPC chair of SSDL/FDL 2000 and the TPC co-chair and general co-chair of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, in 2004 and 2005, respectively. Since December 2002, he has been a Subject Area Editor for the *Journal of System Architecture*.