Guest Editorial

LOW POWER is becoming the holy grail of modern microelectronics, and power consumption is widely recognized as one of the most serious candidate showstoppers for CMOS scaling. The International Symposium on Low-Power Electronics and Design (ISLPED) has been, for the past nine years, one of the most successful forums for presenting and discussing the most significant trends and advances in this highly dynamic field.

With age, ISLPED has matured considerably. The initial focus on low-level design and circuits has widened considerably to embrace architecture and system-level design issues, and the number of submissions has grown steadily. Luckily, the symposium has retained some of the most positive features of its youth: an informal setting, heated discussions, a multidisciplinary flavor, openness to new ideas, and different research fields.

This Special Issue, dedicated to ISLPED 2001, showcases a small set of carefully selected extended versions of papers presented at the symposium (already a very small percentage of the submissions). Extended version submissions were invited after recommendation from session chairs and co-chairs, and each submitted paper went through a careful, multipass, review process. As a result, we believe we have distilled, with much effort from the authors and a number of very competent reviewers, a set of excellent papers, which cover almost completely the wide range of ISLPED current topics of interest.

The first paper, by Im *et al.* focuses on circuit and technology modeling. A compact analytical model of variable threshold voltage CMOS (VTCMOS) is proposed to study the active "on" current, linking it with the standby off-current characteristics. Short channel effects are taken into consideration and their impact on VTCMOS performance is assessed. The second paper, by Moon *et al.* describes a novel-design technique for harmonic resonant rail drivers, which uses only discrete passive components and no external dc power supply. The approach described in this paper could be used to implement an ultra-low-power clock, which dissipates only a small fraction of its standard-CMOS counterpart at the same frequency. Clock-related power is also one of the motivating concerns for the third paper, authored by Zyuban. This paper covers several interesting issues in the design of latches and flip-flops for low-power applications, including optimal transistor sizing and scan chain design for a target power-performance tradeoff point.

The next two papers can be grouped together, as they focus on processor architecture optimization for low power. Both papers target the power consumed by the instruction fetch and dispatch pipeline in high-performance processors. The paper by Ponomarev *et al.* proposes circuit and logic-level techniques to reduce, by as much as 75%, the power consumed by the out-of-order issue queue in superscalar processors. Solomon *et al.* introduce a micro-operation cache, designed to reduce power consumed in the processor's front-end without performance degradation. The micro-operation cache stores instructions in predecoded form and eliminates the need for repeatedly decoding variable length instructions.

Power reduction in processor-based embedded systems is the main objective of the papers by Pouwelse *et al.* and Mamidipaka *et al.* The former takes a system-level perspective and proposes an advanced power-management technique, which schedules tasks and dynamically adjusts the supply voltage of a core processor according to its workload to minimize power, while maintaining adequate performance levels. The latter paper proposes an adaptive address encoding scheme which can significantly reduce the switching activity on highly loaded data address buses.

The last paper in the Special Issue focuses on the analog front-end of tightly power-constrained wireless systems. Mostafa *et al.* describe a fully CMOS variable-gain amplifier (VGA) for GSM receivers. Thanks to its low-power consumption and high accuracy, this amplifier can be used in the feedback path of automatic gain control (AGC) receiver blocks.

Overall, the Special Issue covers a wide range of topics in low-power digital and analog circuits, and processor architecture. We believe that a substantial number of readers will find these selected papers both useful and enlightening.

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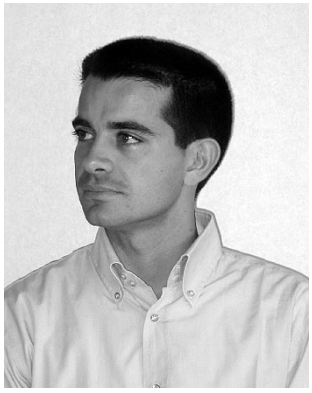
Dr. De has served as a Panelist on the International Electron Devices Meeting (IEDM) and VLSI Test Symposium and Structural Insulated Panels (SIPS). He served as Technical Program Chair of the 2001 ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED'01), as General Chair of ISLPED'02, as Technical Program Chair of 2002 ACM Great Lakes Symposium on VLSI, and as Technical Program Vice Chair of the 2003 International Symposium on Quality Electronic Design (ISQED). He has served on technical program committees of advanced research in VLSI (ARVLSI) and ISQED conferences. He received the Best Paper Award at the 1996 International ASIC Conference, Portland, OR.



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Dr. Benini is a Member of the organizing commitee of the International Symposium on Low-Power Design and of the Design Automation and Test in Europe Conference. He is a Member of technical program committees of several technical conferences, including the Design Automation Conference, International Symposium on Low-Power Design, and the Symposiom on Hardware-Software Codesign.