Guest Editorial System-Level Interconnect Prediction

AS in the past two special sections of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS on system-level interconnect prediction (SLIP) (in the December issues of 2000 and 2001), there are strong contributions in the areas of system level performance modeling and also on the theoretical underpinnings of these models. This year, reflecting their growing commercial importance, there are also two excellent contributions from industry on the application of SLIP techniques to the design of Programmable Logic Devices (PLDs). We begin this special section with a group of two papers and one brief paper on the estimation of system-level performance. The GSRC Technology Extrapolation System (GTX), described in the first paper by Cao *et al.*, offers a unique *a la carte* approach for the specification and comparison of alternative modeling choices. It describes several prepackaged rule chains, but the distinguishing feature of GTX is that users can write their own modules based on GTX data types and grammar. The first brief paper by Christie and Pineda de Gyvez discusses prelayout interconnect yield prediction. Although, the probability of defect formation in a given region of a layout depends on the specific details of the local wiring layout, the overall yield is determined by integrating these probabilities over the whole die area. This makes interconnect yield estimation an especially promising candidate for the SLIP techniques described in this brief. The second paper by Wildman *et al.*, describes a method for defining interconnect geometries that are optimal in the trade off between competing system-level performance objectives. These design solutions are termed Pareto optimal and they form a bounding line between suboptimal and infeasible designs. A Pareto genetic algorithm is used to explore the optimal design of a seven-layer interconnect geometry with respect to yield, power dissipation per cycle, and cycle time. The following two papers form the theoretical group within the special section and are concerned with the improvement in the accuracy of "Rentian" wire length distribution estimates. By this we mean that, over some specified range of partition sizes, the number of terminals required for communication by a group of gates follows a power-law functionality, known as Rent's rule. The paper by Dambre *et al.* provides a thorough exploration of how the different methods of extracting and parameterizing this terminal-gate relationship affect the accuracy of average wire-length estimates. The following paper by Stroobandt provides an overview of a multiterminal net model for hierarchically placed cells. The new approach splits nets into two-terminal segments and develops a technique based on a generating polynomial representation of the segment lengths to correctly calculate the Steiner length of the reconstructed net. The generating polynomial representation allows all possible net segment length combinations to be computed in an efficient manner and results in a net length averaged over all equally likely routing alternatives. The final two contributions to the special section are on the application of SLIP techniques to the optimal design and layout of programmable logic devices. The paper by Rahman *et al.* addresses methods for the design of an SRAM-based programmable gate array routing architecture. It proposes an optimal design in which the range of predefined wire lengths approximates the wire length distribution estimate of a representative netlist. The problem is thus transformed into a Rentian wire length estimation problem. Since it is based on an analytical model, the extension of the analysis to the design of three-dimensional (3-D) architectures with 3-D routing switches is also considered. The final brief by Hutton *et al.* addresses the problem of timing driven placement in the context of PLDs. The place and route problem for PLDs differs from that for ASICs principally because the wiring resources of PLDs are preallocated. Thus, the cost of wires is essentially free up to a fixed line count, and infinitely expensive beyond that point. Moreover, the delays are more predictable because wire sizing and buffering are fixed. This inherent predictability of PLDs, and the very hierarchical nature of the commercial architecture chosen for investigation, are utilized to develop a new algorithm for placement which estimates possible delays based on the statistical characteristics of previously placed netlists. The basic algorithm is implemented in the form of an adaptive loop, which permits tuning of the parameters by combining pessimistic and typical estimators. In conclusion, the papers gathered within this special section represent the state-of-the-art in SLIP, provided by leading researchers from both academia and industry. I have no doubt that these contributions will strengthen the much-needed interaction between interconnect technology and design and I hope they will provide inspiration for future research endeavors.

PHILLIP CHRISTIE, *Guest Editor*
Philips Research Laboratories
Kapeldreef 75, Leuven 3001, Belgium

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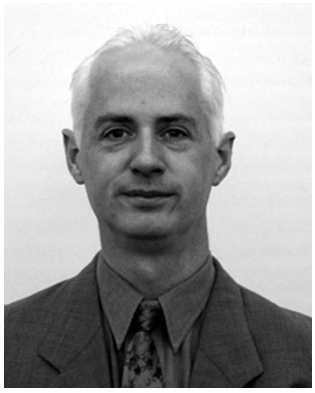

Phillip Christie (M'87) received the B.Sc. and Ph.D. degrees from the School of Engineering and Applied Science, University of Durham, U.K., in 1982 and 1985, respectively.

From 1986 to 1987, he was a Visiting Scientist in the Electrical & Computer Engineering Department at the University of Delaware, Newark, where he worked on applications of Ga-on-Si heteroepitaxy to intracomputer optical interconnects. In 1987, he joined the faculty of the University of Delaware, where his research interests focused on system-level interconnect prediction, multilevel interconnect technology, and the design of test structures for interconnect metrology. In 2001, he joined Philips Research Laboratories,Leuven, Belgium, where he applies system-level interconnect prediction techniques to the development of advanced CMOS technologies.

Dr. Christie was the General Chair of the Third IEEE/ACM Workshop on System-Level Interconnect Prediction in 2001.